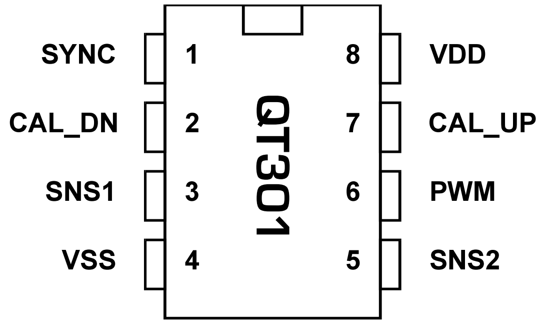
QT301

CAPACITANCE TO ANALOG CONVERTER

- Capacitance to Analog Converter (CAC) IC
- Patented charge-transfer conversion method
- Sub-ranging Direct-to-Analog conversion
- Rescaleable PWM: wide dynamic range
- End-to-end calibration (gain, span) via CAL pins
- 100 kHz PWM
- Spread spectrum acquisition bursts for low noise
- Sample on demand via Sync pin
- Only one external sample capacitor



APPLICATIONS

- **Fluid level sensors**
- **Proximity sensors**
- **Moisture detection**
- **Position sensing**
- **Transducer driver**
- **Material sensors**

The QT301 charge-transfer (QT) IC is a self-contained Capacitance-to-Analog-Converter (CAC) capable of detecting femotofarad level changes in capacitance. This part is designed primarily for stand-alone instrumentation applications.

Primary applications include fluid level sensors, distance sensors, material detectors, transducer amplifiers for pressure and humidity sensing functions, and other uses requiring quantified capacitance data.

Unlike other Quantum products, the QT301 does not process its acquired data. Its only output is raw, unprocessed data in filterable PWM form that can be translated into an analog voltage by a simple RC network. This allows the designer to treat the device as a CAC for measurement applications.

The PWM range is set via two inputs that control the starting and ending point of the conversion range. For example, if the capacitance range of Cx is from 27pF to 38pF, the QT301 can be calibrated so that the PWM zero point occurs at 27pF, and the endpoint (255) occurs at 38pF. In this way, the PWM range is optimized for the zone of interest. These calibration points are stored in internal EEPROM and do not have to be reacquired after a power reset. This means that the resolution of the part can be compared easily to other methods that might otherwise require 12 or more bits of overall resolution.

The device operates on demand via a sync input pin. The sync input can also be used to avoid external noise sources and cross-interference from adjacent QRG capacitive sensors. Unique among capacitance sensors, this device features spread-spectrum burst modulation, permitting extremely high noise rejection characteristics for very robust signals even in high EMI environments.

The device requires only a single sampling capacitor (Cs) to acquire signals. The value of this capacitor controls the gain of the sensor, and it can be adjusted over 2½ decades of range from 1nF to 500nF. No external switches, opamps, or other components are required.

AVAILABLE OPTIONS

T_A	SOIC	8-PIN DIP
0^0C to $+70^0$C	-	QT301-D
-40^0C to $+85^0$C	QT301-IS	-

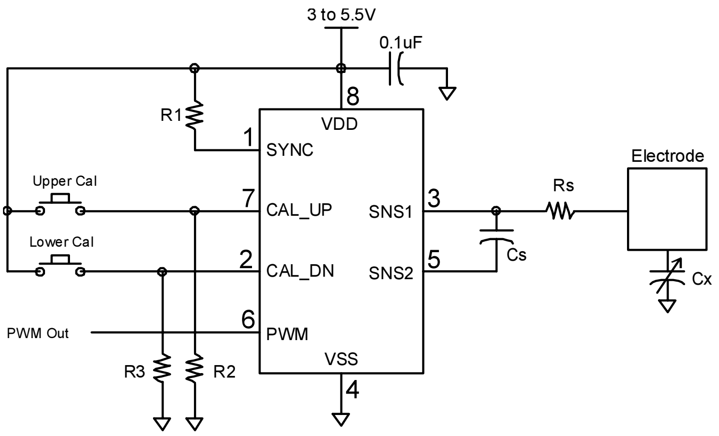
1 - Overview

The QT301 is a digital burst mode charge-transfer (QT) capacitance-to-analog converter (CAC). It has a PWM output designed for applications such as fluid level sensing and distance gauging; the PWM signal is eight bits in resolution. The IC features two calibration inputs for end-to-end span calibration. The output depends on load (Cx) and sampling capacitor (Cs) values.

1.1 Basic Operation

The QT301 has internal EEPROM to store the two calibration points. The sensor acquires the signal from the electrode and calculates the PWM result using the two calibration points. The sensor can be calibrated via the two calibration inputs (see Section 4). The signal can be acquired either continuously or it can be synchronized on an external signal. The response time of the PWM depends largely on the acquisition burst spacing.

Figure 1-1 Basic Circuit Diagram



1.2 Basic Circuit

Figure 1-1 shows a basic circuit diagram for the QT301. The pin layout of the QT301 is as explained in Table 1-1. In this particular circuit, C1 should be 100nF and R1, R2 and R3 should all be 10K.

R1 is only required if the synchronization feature is not used and can be connected to either VDD or VSS.

Cs should be between 1nF and 500nF depending on the sensitivity required. Use either NPO or PPS capacitors for best results.

Rs is calculated with the following formula:

$$Rs < \frac{166 \times 10^3}{Cx}$$

where Cx is expressed in pF.

Table 1-1 Pin Description

Pin	Name	Function
1	SYNC	Sync Input
2	CAL_DN	Lower Calibration input
3	SNS1	Sense 1 line (to electrode)
4	VSS	Negative supply (ground)
5	SNS2	Sense 2 line
6	PWM	PWM output
7	CAL_UP	Upper Calibration input
8	VDD	Positive supply

2 - Signal Acquisition

The QT301 has a power-up delay of 300ms. During this interval it does not acquire signals or generate a PWM result; it also ignores calibration inputs. This delay helps to prevent false calibrations due to signal noise on Vdd during startup.

Figure 2-1 shows the basic QT301 acquisition timing parameters. Tbd is the burst duration, Tbs is the burst spacing from the start of one burst to the start of the next burst; when there is no Sync signal Tbs = Tbd+2.5ms.

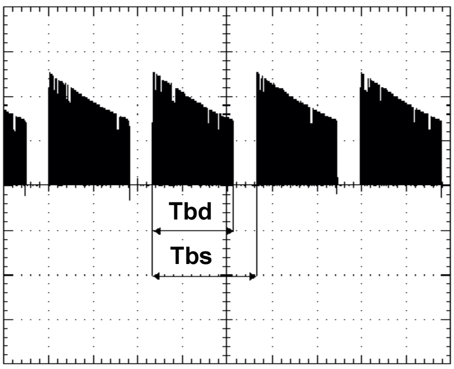
2.1 Burst Properties

The QT301 employs bursts of charge-transfer cycles to acquire its signal. Burst mode dramatically reduces RF emissions and lowers susceptibility to EMI.

The acquisition burst operates in a band between 230kHz and 310kHz. The burst is spread-spectrum modulated within this band to suppress interference from external noise sources.

The QT switches and charge measurement hardware functions are all internal to the QT301. A 16-bit single-slope switched capacitor, analog to digital converter (ADC), includes both the required QT charge and transfer switches in a configuration that provides direct ADC conversion. The ADC is designed to dynamically optimize the QT burst length according to the rate of charge buildup on Cs, which in turn depends on the values of Cs, Cx, and VDD. VDD is used as the charge reference voltage.

Figure 2-1 Acquisition Burst: No Sync Pulse



2.2 CS / CX Dependency

The signal value is a direct function of Cs and Cx, where Cs is the fixed sample capacitor, and Cx is the unknown capacitance. These two values influence device sensitivity, resolution and response time, making them very important parameters.

Sensitivity and resolution are also a function of the size, shape, and composition of the electrode, the composition and thickness of any dielectric overlaying the electrode, the composition and aspect of the object being sensed, and the degree of mutual coupling between the electrode and the object being sensed.

2.3 Burst Length

The burst length (and hence the signal level) is described by the following formula:

$$BL = \frac{k \cdot C_S}{C_X}$$

Where 'k' is a constant, typically 0.51 (this may vary slightly from device to device).

Each doubling of Cs increases the signal level and differential sensitivity by a factor of two. Likewise, doubling Cx reduces the signal level and differential sensitivity by a factor of two (Figures 6-1, 6-2, page 8).

The device has an internal Cx, Csns, which adds to the Cx in the formula. This capacitance is about 11pF.

Because the QT301 has an 8-bit PWM output which spans two calibration endpoints, the PWM output value is expressed as:

$$PWM = 255 \cdot \frac{\frac{k \cdot C_S}{C_X} - \frac{k \cdot C_S}{C_{X1}}}{\frac{k \cdot C_S}{C_{X2}} - \frac{k \cdot C_S}{C_{X1}}} = 255 \cdot \frac{C_{X2} \cdot (C_{X1} - C_X)}{C_X \cdot (C_{X1} - C_{X2})};$$

where:

Cx1 is the capacitance at the lower cal point
Cx2 is the capacitance at the upper cal point, and
Cx is the measured capacitance between Cx1 and Cx2

Particularly noteworthy is that Cs is not part of this equation; the PWM result is purely a function of the three Cx values. Cs only needs to be large enough to prevent granularity problems (i.e. coarseness or resolution).

In most cases the result is a nearly-linear response between the endpoints. Only when the capacitance of the lower cal point becomes comparable to delta Cx does the result become substantially non-linear.

For a linear response, make sure that the lower cal point capacitance is significantly larger than the delta capacitance between the endpoints. If the delta Cx amounts to 5pF, the response will be accurate to 2.4% of full scale if the lower cal point is 50pF. But if the lower cal point is only 20pF and the delta Cx is 10pF, the error rises to 10% at points. The largest errors occur near the middle of the Cx span.

An example of the error can be seen in Figure 2-6.

Non-linear errors can be linearized using polynomials or a piece-wise linear correction method in a microcontroller. A spreadsheet with the calculations for this equation and the error terms can be obtained on request.

Figure 2-2 Acquisition Burst with Sync Signal

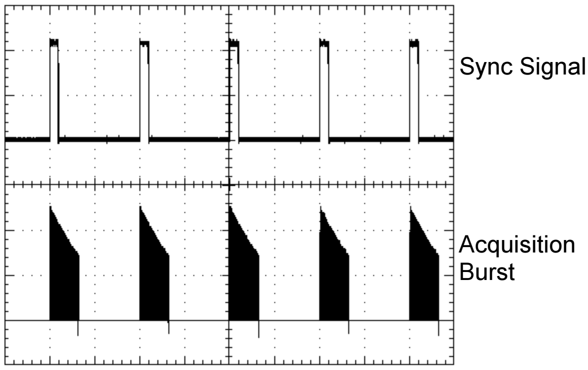


Figure 2-3 Acquisition Burst: Sync Lost

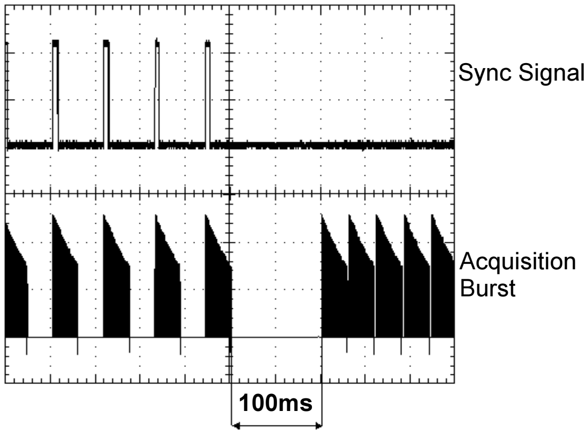


Figure 2-4 Acquisition Burst: Sync Reacquired

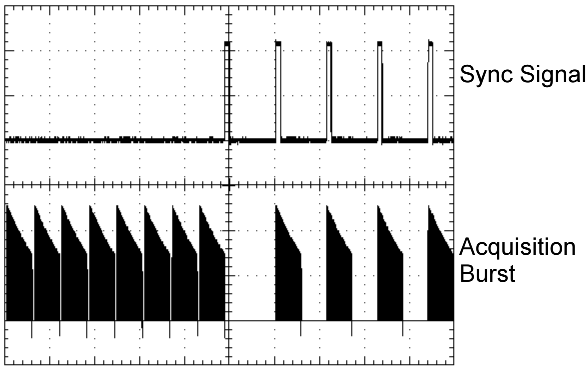
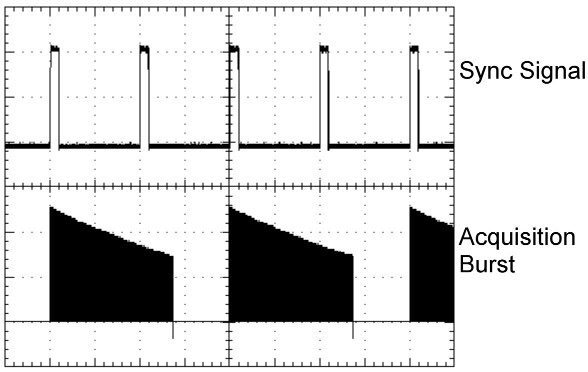


Figure 2-5 Sync Overclocked



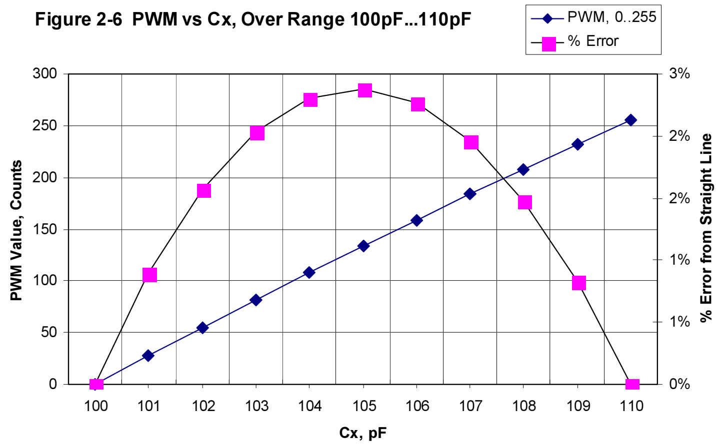


Figure 2-6 PWM vs Cx, Over Range 100pF...110pF

2.4 Sync Input

Bursts can be synchronized to external noise sources such as powerline fields to suppress their interfering effects. A typical sync circuit is shown in Figure 2-7. By synchronizing with a noise source, the noise itself becomes highly correlated with the acquired data, and AC alias components effectively disappear from the signal. Synchronization works best on low frequency, highly repeatable signals, such as mains frequency (50/60 Hz) sources.

Figure 2-2 shows the effect of sync pulses on the burst rate. A sync signal triggers a burst on the rising edge.

There is a Sync timeout of 100ms as shown in Figure 2-3. If Sync pulses cease for >100ms, the Sync signal will be treated as being lost and the device will start to acquire at its own default rate again. When using the Sync feature it is important that the Sync pulses are spaced less than 100ms apart.

Figure 2-2 shows the acquisition burst in relation to Sync pulses. If no rising edge is detected for 100ms, the QT301 will revert to the default timing shown in Figure 2-1. Figure 2-4 shows the sudden start of a train of Sync pulses and the effect on the acquisition bursts.

Should the sync signal overclock the acquisition bursts (Figure 2-5), the device will trigger on the next rising edge after a delay of Tbd+2.5ms.

The 2.5ms is the minimum gap between bursts is to allow Cs to properly discharge; Sync is not possible during this interval nor is it possible to re-sync during a burst.

3 PWM Output

The PWM output is a 100KHz ±7% square wave. It can be filtered using a simple RC circuit, or fed directly into a timer circuit that can measure its duty cycle with sufficient resolution. If an RC is used, the resistor should be at least 10K ohms to reduce pin loading errors.

The PWM duty cycle is defined as follows:

$$D_{PWM} = \frac{T_{PWM\_high}}{T_{PWM\_Period}}$$

If an RC circuit is used, it is often best to put a voltage follower circuit on the output of the filter to buffer the output voltage (Figure 2-7).

Note that the PWM output is not 100% linear with changes in Cx capacitance from end to end. The transfer function for the QT301 vs Cx is described in Section 2.3.

During CAL, the PWM output value is locked in place with the value just prior to when the CAL process was triggered. Only after CAL is complete is the PWM updated with the new results.

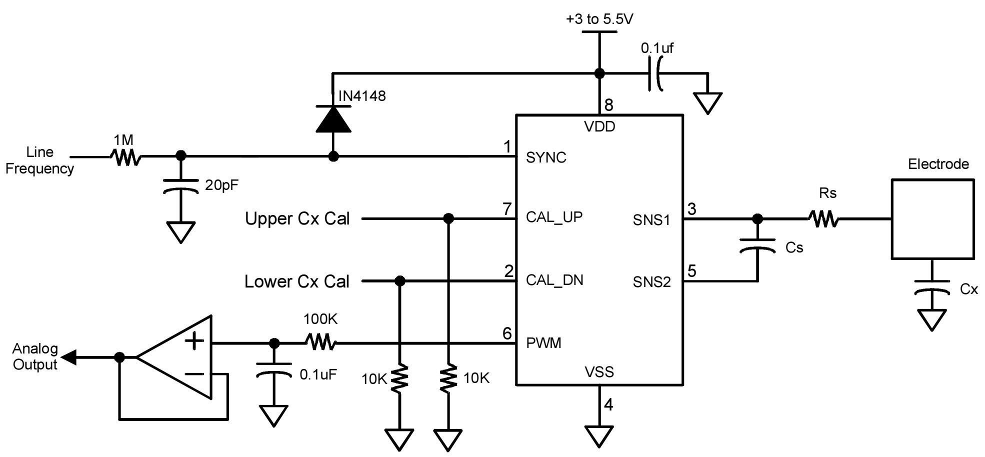
4 Calibration

The QT301 should be calibrated end to end to have an effective, properly scaled PWM output. The calibration is done on a 'learn by example' basis. Each end is calibrated separately while the appropriate end-point signal level is applied. After the Cal process, the PWM signal will scale itself to reflect these endpoints with the best resolution possible.

4.1 Calibration Pins

The CAL_DN pin should be used to calibrate the signal when the electrode is at its lowest level of Cx, for example with a level probe when the fluid is at a minimum.

Figure 2-7 Line Sync and PWM Output Filter



The CAL_UP pin should be used to calibrate the signal when the electrode is at its maximum useable level of Cx, for example with a level probe when the fluid is at the top.

It does not matter whether CAL_DN or CAL_UP are applied first. After calibration is complete, either CAL_DN or CAL_UP can be asserted again to obtain a fresh calibration for the corresponding end point, without affecting the other end point.

4.2 Calibration Process

The CAL pins are inputs used to trigger a CAL process on the upper (max Cx) or lower (min Cx) capacitance endpoints. These pins must be pulled low via a pulldown resistor on each, to prevent damage.

To calibrate either endpoint, assert either CAL pin high using an open-source output from a mosfet or microcontroller, or, a collector from a PNP transistor whose emitter is connected to Vdd. Hold this level high for 2.5ms minimum (preferably, 3ms to be safe). Then release the pin to try to float down.

The QT301 will continue to hold the pin high starting at the 2.5ms point. There should be no contention problem with an external voltage plus the QT301 both holding this pin high.

When the QT301 is done calibrating, it will release the CAL pin in question to float low. A host controller can use this feature to check when the calibration process has completed.

Calibration takes 15 acquisition burst samples to complete. The new calibration data is stored in internal EEPROM when the host releases the CAL pin to float low again; the chip also begins to operate normally again at this time.

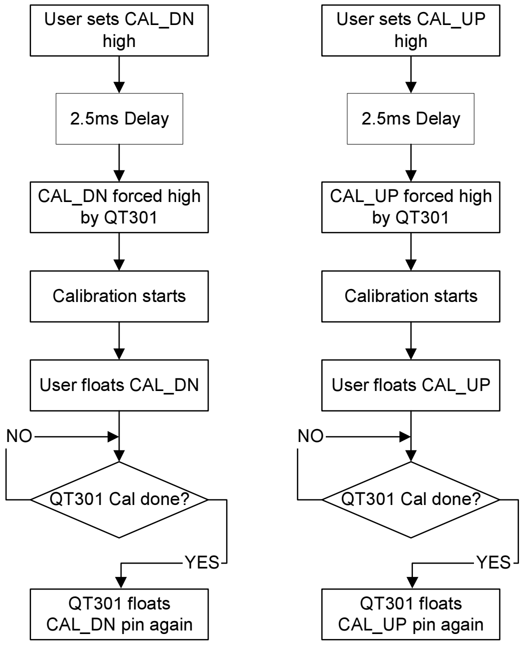
Figure 4-1 shows the control flows for calibration.

The capacitive signal on the electrode should be as stable and noise-free as possible during the CAL intervals to ensure accurate calibration points.

During a CAL cycle, the PWM output functions normally using the last known good calibration data and signal value. The PWM output will change again only when the CAL process is complete.

Note: The CAL pins should never be driven low. Driving either of the CAL pins low will short circuit the chip.

Figure 4-1 Calibration Process



5 - CIRCUIT GUIDELINES

5.1 Sample Capacitor

The charge sampler capacitor (Cs) can be virtually any plastic film or low to medium-K ceramic capacitor. The acceptable Cs range is from 1nF to 500nF depending on the sensitivity required; larger values of Cs demand higher stability to ensure reliable sensing. Acceptable capacitor types include plastic film (especially PPS film) and NP0/C0G ceramic. X7R ceramic can also be used but this type is less stable over temperature.

5.2 Power supply, PCB Layout

The QT301 makes use of the power supply as a reference voltage. The acquired signal will shift slightly with changes in VDD; fluctuations in VDD often happen when additional loads are switched on or off such as LEDs etc.

Care should be taken when designing the power supply, as any change in VDD will affect the PWM level.

If the power supply is shared with another electronic system, make sure the supply is free of spikes, sags, and surges. The supply is best locally regulated using a conventional 78L05 type regulator, or almost any 3-terminal LDO device from 3V to 5V.

For proper operation, a 0.1µF or greater bypass capacitor must be used between VDD and VSS; the bypass cap should be placed very close to the device pins. The PCB should if possible include a copper pour under and around the IC, but not extensively under the SNS pins or lines.

5.3 ESD Protection

In cases where the electrode is placed behind a dielectric panel the IC will be protected from direct static discharge. However, even with a panel transients can still flow into the electrodes via induction, or in extreme cases via dielectric breakdown. Porous materials may allow a spark to tunnel right through the material. Testing is required to reveal any problems.

The device has diode protection on its SNS pins that absorb most induced discharges (up to 20mA), and protect the device. The usefulness of the internal clamping will depend on the dielectric properties, panel thickness, and rise time of the ESD transients. In extreme cases, ESD dissipation can be aided further by adding a resistor in series with the electrode.

The charge pulse can be a minimum of 1µs and therefore the circuit can tolerate values of series-R up to 18k in cases where electrode Cx load is below 10pF. Extra diode protection may be used at the electrodes but this often leads to additional RFI problems as the diodes will rectify RF signals into DC; this will disturb the sensing signals. Series-R's should be low enough to permit at least six RC time-constants (i.e. a net RC timeconstant of 1/6 µs) to occur during the charge pulse, where R is the added series-R and

C is the load Cx. If the series-R or Cx is too large, sensitivity will be reduced.

Directly placing semiconductor transient protection devices or MOV's on the sense leads is not advised; these devices have extremely large amounts of non-linear parasitic C, which will swamp the capacitance of the electrode and may deliver spurious sensing results.

5.4 RF Susceptibility

PCB layout, grounding, and the structure of the input circuitry have a great bearing on the success of a design that can withstand strong RF interference. The circuit is remarkably immune to RFI provided that certain design rules are adhered to:

1. Use SMT components to minimize lead lengths.
2. Connect electrodes to SNS1, not SNS2.
3. Use a ground plane under and around the circuit and along the sense lines, that is as unbroken as possible except for relief under and beside the sense lines to reduce total Cx. Relieved rear ground planes along the SNS lines should be ‘mended’ by bridging over them at 1cm intervals with 0.5mm ‘rungs’ like a ladder.
4. Ground planes and traces should be connected only to a common point near the VSS pin of the IC.
5. Route sense traces away from other traces or wires that are connected to other circuits.
6. Sense electrodes should be kept away from other circuits and grounds which are not directly connected to the sensor’s own circuit ground; other grounds will appear to float at high frequencies and couple RF currents into the sense lines.
7. Keep the Cs sampling capacitors and all series-R components close to the IC.
8. Use a 0.1µF minimum, ceramic bypass cap very close to the VSS/VDD supply pins.
9. Use series-R’s in the sense line of as large a value as the circuit can tolerate without degrading sensitivity appreciably (see Section 1.2).
10. Bypass input power to chassis ground and again at circuit ground to reduce line-injected noise effects. Ferrites over the power wiring may be required to attenuate line injected noise.

Achieving RF immunity requires diligence and a good working knowledge of grounding, shielding, and layout techniques. Very few projects involving these devices will fail EMC tests once properly constructed.

6 Electrical specifications

6.1 ABSOLUTE MAXIMUM SPECIFICATIONS

Operating temp. as designated by suffix
Storage temp. -65°C to +125°C
Vdd. -0.5 to +6V
Max continuous pin current, any control or drive pin. . . . . ±40mA
Short circuit duration to ground, any pin. . . . . infinite
Short circuit duration to VDD, any pin. . . . . infinite
Voltage forced onto any pin. . . . . -1V to (VDD + 0.5) Volts

6.2 RECOMMENDED OPERATING CONDITIONS

Vdd. +3 to 5V
Short-term supply ripple+noise. . . . . ±5mV
Long-term supply stability. . . . . ±100mV
Cs value. 1 to 500nF
Cx value. 0 to 500pF

6.3 GENERAL SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Notes
E_{WC}	EEPROM write cycles	100,000				
T_{PU}	Power up time		300		ms	
Csns	Sensor pin internal capacitance		11		pF	
K	Burst length coefficient		0.51			

6.4 AC SPECIFICATIONS

VDD = 3.3 Volts, Cs = 100nF, Cx = 5pF, Ta = recommended range, unless otherwise noted

Parameter	Description	Min	Typ	Max	Units	Notes
T_{PC}	Charge/transfer time	1	1.25	1.5	µs	+/-10% over voltage and temperature range
F_C	Burst center frequency		265		kHz	
F_D	Burst frequency modulation		±7		%	
T_{BD}	Burst length		16		ms	
T_{BS}	Burst spacing	T_{BD} + 2.5		T_{BD} + 100	ms	
F_{PWM}	PWM frequency		100		kHz	
T_{CPD}	Calibration pulse duration	2.5			ms	
T_{CD}	Calibration duration		15 x T_{BS}		ms	

6.5 DC SPECIFICATIONS

VDD = 3.3 Volts, Cs = 100nF, Cx = 5pF, Ta = recommended range, unless otherwise noted

Parameter	Description	Min	Typ	Max	Units	Notes
I_{DD}	Supply current		5		mA	@5V
I_{DD}	Supply current		2.9		mA	@3.3V
V_{IL}	Input low voltage			0.3 VDD	V	VDD = 3 to 5.5V
V_{IH}	Input high voltage	0.6 VDD			V	VDD = 3 to 5.5V
V_{OL}	Low output voltage			0.5	V	I_{OL} = 6mA
V_{OH}	High output voltage	VDD-0.7			V	I_{OH} = -1.5mA
A_R	Acquisition resolution		11		bits	
S	Resolution per bit		8		fF	

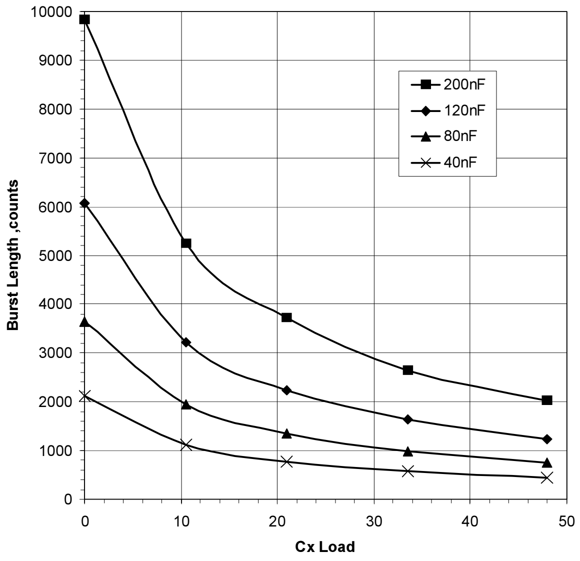


Figure 6-1 Typical Burst Length versus Cx & Cs; VDD = 5.0 Volts

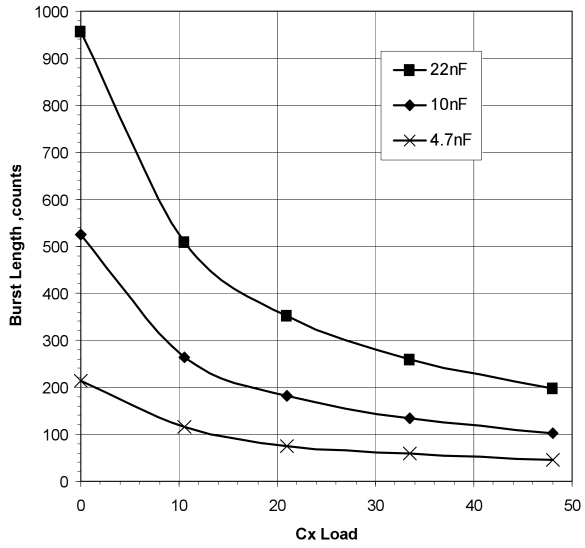


Figure 6-2 Typical Burst Length versus Cx & Cs; VDD= 5.0 Volts

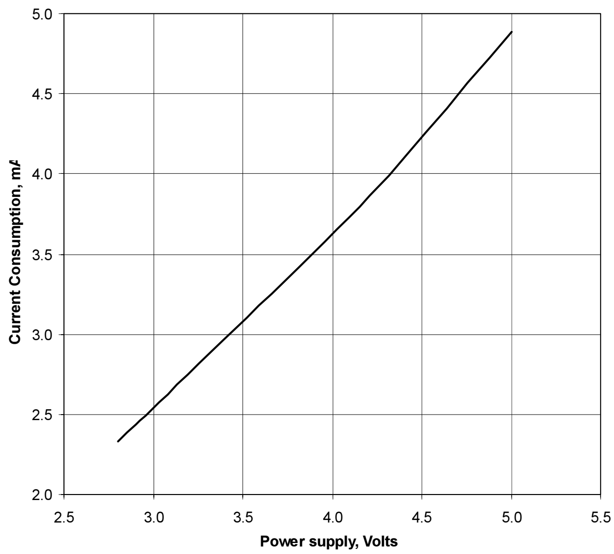


Figure 6-3 Power Consumption versus VDD

Figure 6-4 Typical Signal Deviation versus Temperature
VDD = 5.0 Volts, Cx = 10pF

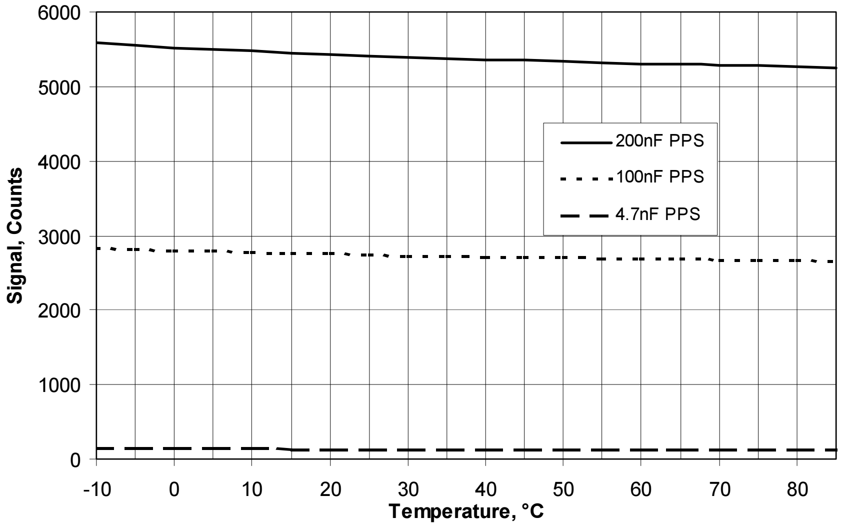
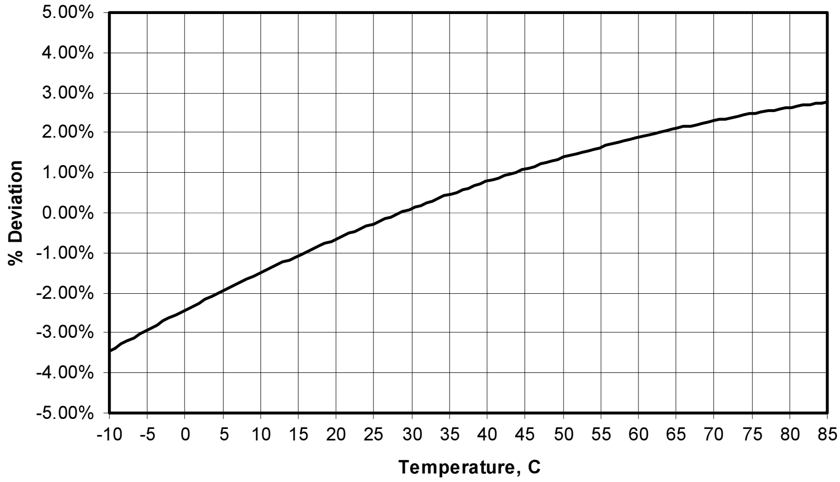
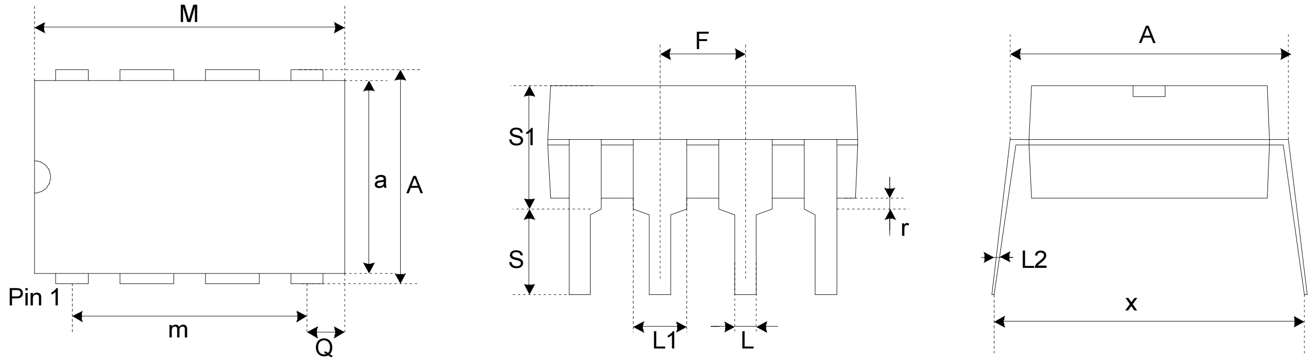
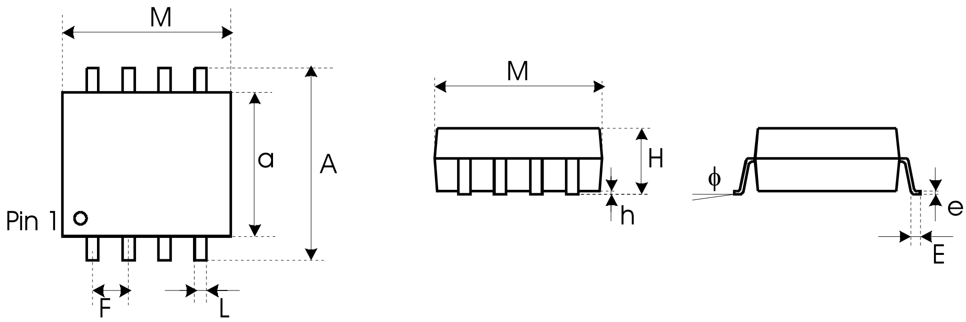


Figure 6-5 Typical Signal Deviation vs. Temperature
Vdd = 5.0 Volts, Cx = 10pF, Cs = 5nF - 200nF PPS Film





Package type: 8-pin Dual-In-Line						
Symbol	**Millimeters**			**Inches**		
	Min	**Max**	**Notes**	**Min**	**Max**	**Notes**
a	6.1	7.11		0.24	0.28	
A	7.62	8.26		0.3	0.325	
M	9.02	10.16		0.355	0.4	
m	7.62	-	Typical	0.3	-	Typical
Q	0.69	0.94		0.027	0.037	
L	0.356	0.559		0.014	0.022	
L1	1.14	1.78		0.045	0.07	
L2	0.203	0.305		0.008	0.012	
F	2.54	-	BSC	0.1	-	BSC
r	0.38	-		0.015	-	
S	2.92	3.81		0.115	0.15	
S1	-	5.33		-	0.21	
x		10.9			0.43	



Package type: 8-pin Wide SOIC						
Symbol	**Millimeters**			**Inches**		
	Min	**Max**	**Notes**	**Min**	**Max**	**Notes**
a	5.21	5.41		0.205	0.213	
A	7.62	8.38		0.3	0.33	
M	5.16	5.38		0.203	0.212	
F	1.27		BSC	0.05		BSC
L	0.305	0.508		0.012	0.02	
h	0.102	0.33		0.004	0.013	
H	1.78	2.03		0.07	0.08	
e	0.178	0.254		0.007	0.01	
E	0.508	0.889		0.02	0.035	
ϕ	0°	8°		0°	8°	

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